REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on January 15, 2003, and the references cited therewith.

No claims are amended, canceled, or added; as a result, claims 1-29, and 42-53 remain pending in this application.

§102 Rejection of the Claims

Claims 1-29 and 42-53 were rejected under 35 USC § 102(e) as being anticipated by Ooishi et al. (U.S. 2002/0051404).

Claim 1 recites a delay locked loop (DLL) and a DLL controller having a "selector" for selectively activating a "control signal" during a test mode to "prevent" the DLL from performing a synchronization operation during the test mode.

Ooishi et al. disclose a memory device having elements different from the elements of claim 1. Further, the elements of Ooishi et al. perform functions different from the functions of the elements of claim 1. Ooishi et al. disclose an adjustment circuit 200 (FIG. 1) to switch a frequency of an internal clock int.CLK to a higher frequency during a test mode to reduce the test time.

FIG. 2 of Ooishi et al. shows adjustment circuit 200 having transmission gates to select between an external clock signal CLK (FIG. 1) and a signal at the output of an generation circuit 202 to generate the int.CLK signal. Generation circuit 202 operates when transmission gate 204 turns on by a test mode signal TM to pass a clock signal CLK from circuit 8 (FIG. 1). The TM signal is activated (high) only in a test mode. Thus, generation circuit 202 only operates in a test mode.

FIG. 5 shows detail of generation circuit 202 including a DLL 300 connected to a conversion circuit 400. During a test mode, DLL 300 receives the CLK signal and generates delay signals CK1-CLK8 based on the timing of the CLK signal. A delay control circuit 330 (FIG. 4) of DLL 300 controls the timing of the CLK1-CLK8 signals. Conversion circuit 400 has logic circuits 402 and 404 for selecting among the CLK1-CLK8 signals to generate an output signal OUT. This OUT signal is the signal at the output of generation circuit 202 (FIG. 2).

During a test mode, generation circuit 202 selects the OUT signal as the int.CLK signal. The frequency of the OUT signal is selected by a combination of switches SW1-SW8. The selection of the switches SW1-SW8 is controlled by mode register 46 of FIG. 1 (paragraph 0089). FIG. 7-FIG. 10 show examples of the OUT signal of FIG. 5 with different frequencies based on different selections of the SW1-SW8 switches.

In the description above, since delay control circuit 330 controls the timing of the CLK1-CLK8 signals based on the timing of the CLK signal, if delay control circuit 330 prevents DLL 300 from performing any operation during the test mode, the relationships between the CLK1-CLK8 signals and the CLK signal would be undefined. Since the OUT signal is generated based on the CLK1-CLK8 signals, if the relationships between the CLK1-CLK8 signals and CLK signal are undefined, the relationship between the OUT and CLK signals is also undefined. Since the int.CLK signal is the OUT signal during the test mode, if relationship between the OUT and CLK signals is undefined, the relationship between the int.CLK and CLK signals is also undefined. FIG. 7 shows one example of the timing relationships between the OUT (int.CLK) and CLK signals. In FIG. 7, for the relationship between the OUT (int.CLK signal) and CLK signals to be defined as shown with exact delay time increment (1/16T) during the test mode, the CLK1-CLK8 signal must be defined. For the CLK1-CLK8 signals to be defined, delay control circuit 330 must allow (not prevent) DLL 300 to perform an operation. Since delay control circuit 330 must allow DLL 300 to perform an operation, Ooishi et al. do not disclose a DLL controller with a selector to "prevent" a DLL from performing a synchronization operation as claimed in claim 1.

Further, the switches SW1-SW8 of Ooishi are only used to select a frequency of the int.CLK (OUT) signal during the test mode. The switches SW1-SW8 are not a "selector" used to activate a "control signal" to prevent the DLL form performing a synchronization operation during the test mode. Therefore, Ooishi et al. do not disclose a "selector" for activating a "control signal" as claimed in claim 1.

Based on the reason presented above, Ooishi et al. do not disclose a DLL controller having a "selector" for selectively activating a "control signal" during a test mode to "prevent" the DLL from performing a synchronization operation during the test mode. Since Ooishi et al. do not disclose all of the elements of the invention as recited in claim 1, this claim is not

anticipated by Ooishi et al. Therefore, Applicant respectfully requests that the rejection of claim 1 be reconsidered and withdrawn and that claim 1 and its dependent claims be allowed.

Independent claims 8, 14, 19, 21, 26, 42, 45, 48, and 51 recite elements similar to the elements of claim 1. For example, claims 8 and 26 recite a DLL, and a DLL controller having a "selector" for activating a DLL control signal during a test mode to "prevent" the DLL from adjusting the delay during the test mode. Claims 14, 19, 48, and 51 recite a DLL, and a DLL controller having a "selector" for activating a DLL control signal during a test mode to "disable" the shifting operation during the test mode. Claim 42 recites a DLL, and a DLL controller having a "selector" for generating a DLL control signal during a test mode to "disable" the synchronization operation during the test mode. Claim 45 recites a DLL having a shift register, and a DLL controller having a "selector" for activating a DLL control signal during a test mode to "prevent" the shift register adjusting the delay during the test mode.

Since independent claims 8, 14, 19, 21, 26, 42, 45, 48, and 51 recite elements similar to the elements of claim 1, these claims are also not anticipated by Ooishi et al. for reasons similar to the reasons presented above regarding claim 1. Applicant requests that the rejection of these claims be reconsidered and withdrawn and that these claims and their dependent claims be allowed.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's representative at (612) 373-6969 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 15 day of April, 2003.

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